

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

TAE-WOO JUNG, ET AL.

Application No.:

Filed:

For: **METHOD FOR FABRICATING
SEMICONDUCTOR DEVICE HAVING
TRENCH TYPE DEVICE ISOLATION LAYER**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

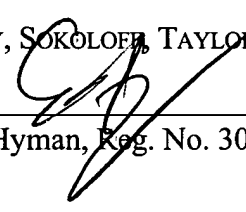
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 30, 2003



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Information Disclosure Statement

New U.S. Patent Application for
**METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
HAVING TRENCH TYPE DEVICE ISOLATION LAYER**

Our Ref. No.: P03H3019/US/cj

Reference No.:

- (1) US Patent No. 6,444,540
- (2) US Patent No. 6,500,727
- (3) US Patent No. 6,218,309
- (4) US Patent No. 6,579,801